



The Value of Activity in Design and Verification

Simulation being a critical component of the design and verification cycle for modern microprocessors and System-on-Chip (SoC) designs

level behaviour from the system level communication activities. This presentation provides an overview of the current status, existing challenges and possible solutions. Furthermore, it discusses various features

09/13/2016

10:00 am

ENB 323

For details of the event

Transport Forum

15th November 2016

10:00 am

ENB 323

www.transportforum.org.uk

www.transportforum.org.uk

Transport Forum

Transport Forum

15th November 2016

10:00 am

ENB 323